FIG. 1

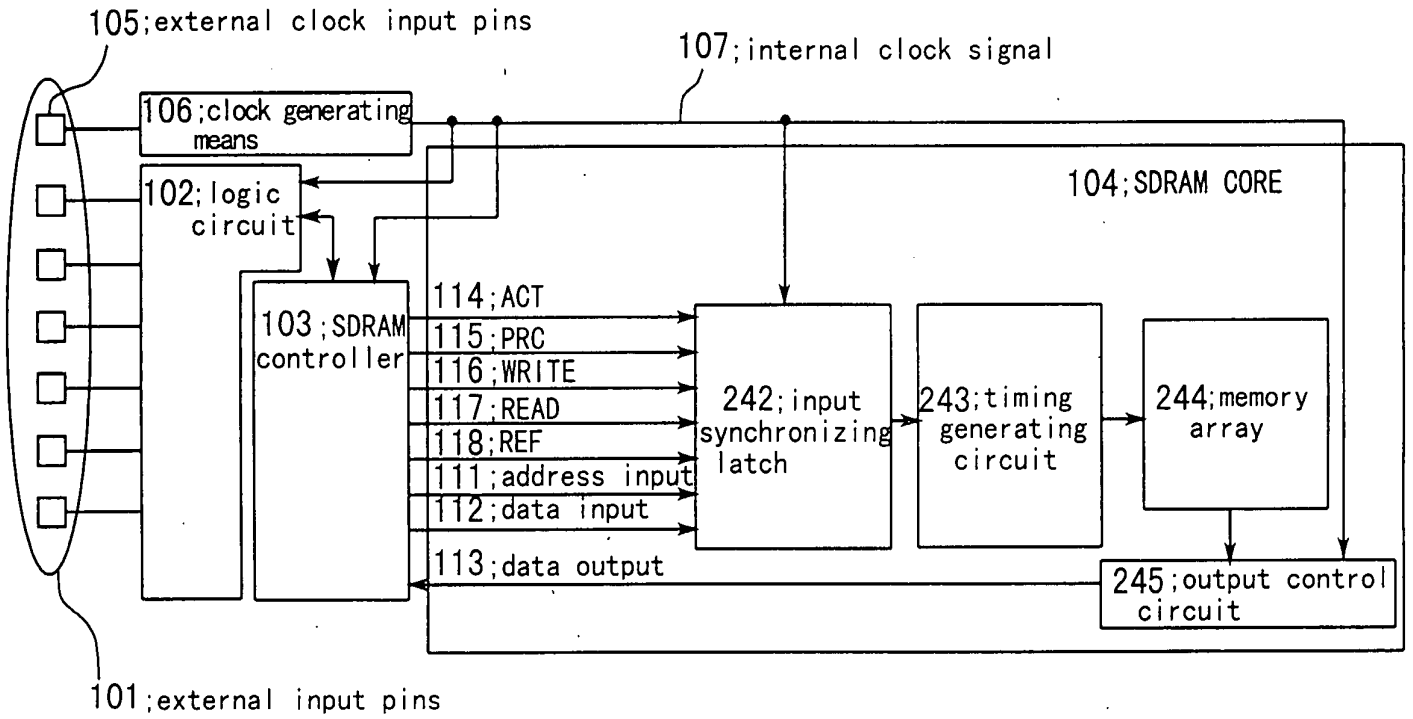
105;external clock input pins
107;internal clock signal
106;clock generating means
102;logic circuit
104;SDRAM CORE
103;SDRAM controller
114;ACT
115;PRC
116;WRITE
117;READ
118;REF
111;address input
112;data input
113;data output
242;input synchronizing latch
243;timing generating circuit
244;memory array
245;output control circuit
101;external input pins

FIG. 2

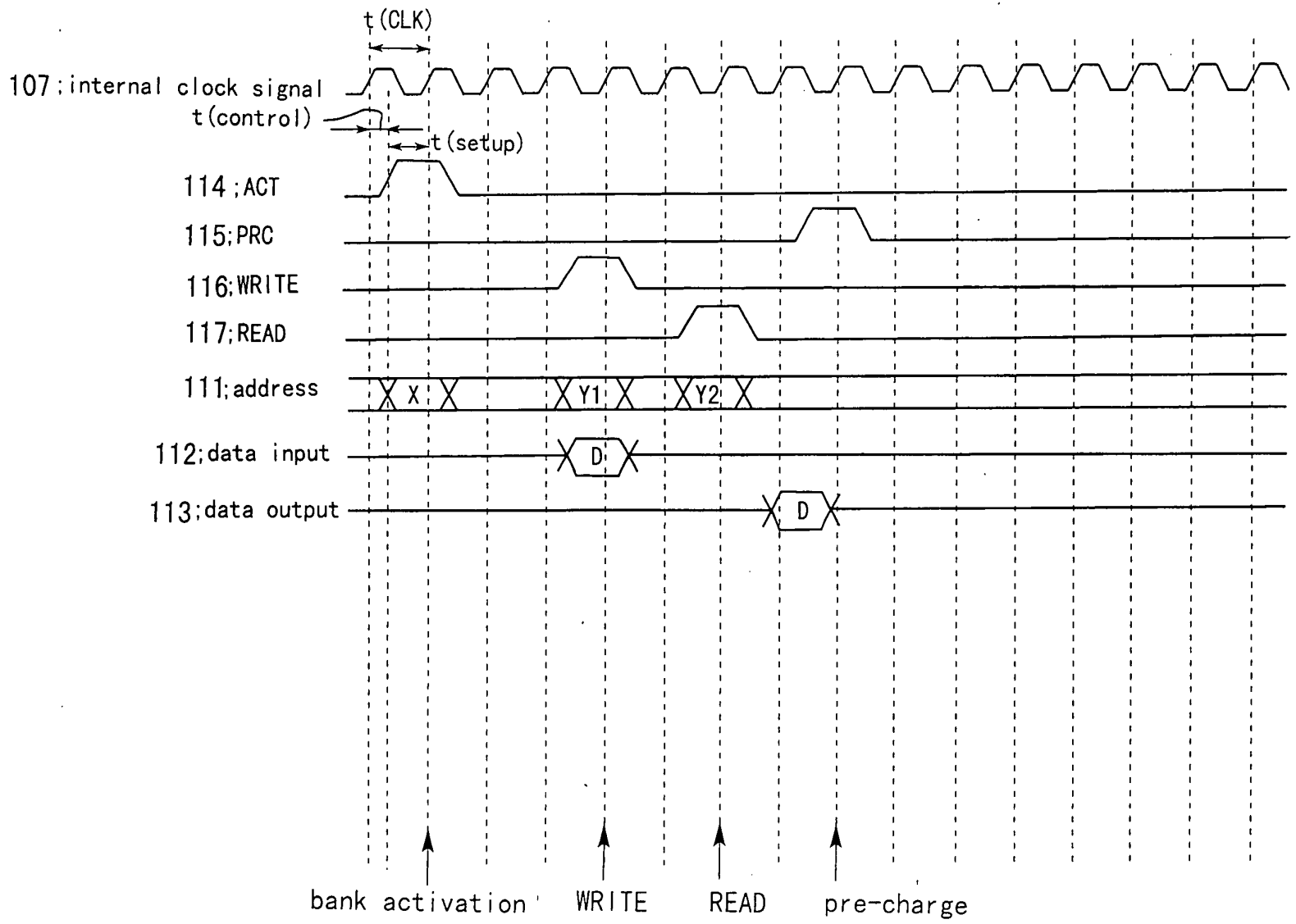
t(CLK)
107;internal clock signal
t(control)
t(setup)
114;ACT
115;PRC
116;WRITE
117;READ
111;address
X
Y1
Y2
112;data input
D
113;data output
D
bank activation
WRITE
READ
pre-charge

FIG. 3

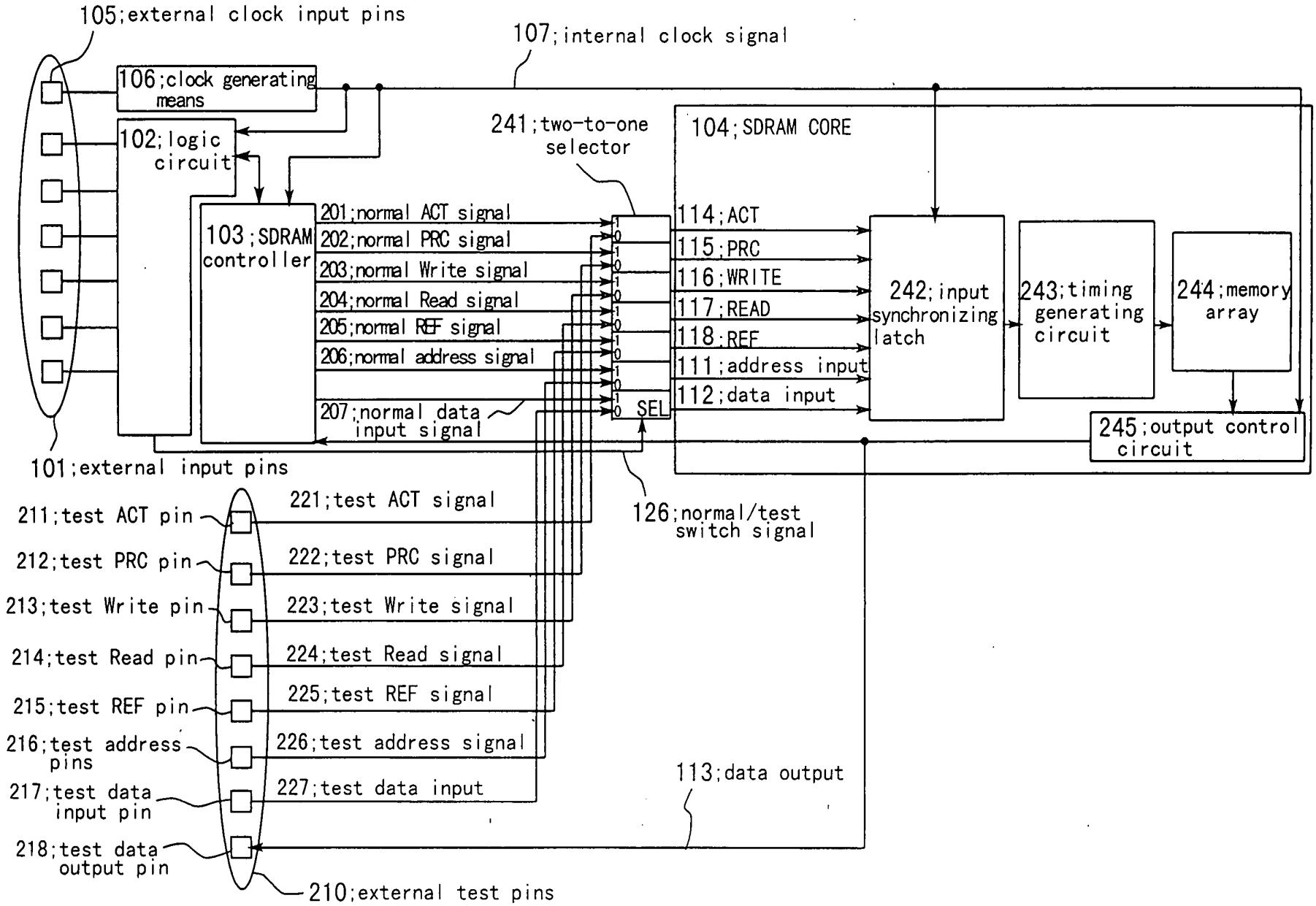
105;external clock input pins
107;internal clock signal
106;clock generating means
102;logic circuit
241;two-to-one selector
104;SDRAM CORE
103;SDRAM controller
201;normal ACT signal
202;normal PRC signal
203;normal Write signal
204;normal Read signal
205;normal REF signal
206;normal address signal
207;normal data input signal
114;ACT
115;PRC
116;WRITE
117;READ
118;REF
111;address input
112;data input
SEL
242;input synchronizing latch
243;timing generating circuit
244;memory array
245;output control circuit
101;external input pins
126;normal/test switch signal
211;test ACT pin
212;test PRC pin
213;test Write pin
214;test Read pin
215;test REF pin
216;test address pins
217;test data input pin
218;test data output pin
221;test ACT signal
222;test PRC signal
223;test Write signal
224;test Read signal
225;test REF signal
226;test address signal
227;test data input
113;data output
210;external test pins

FIG. 4

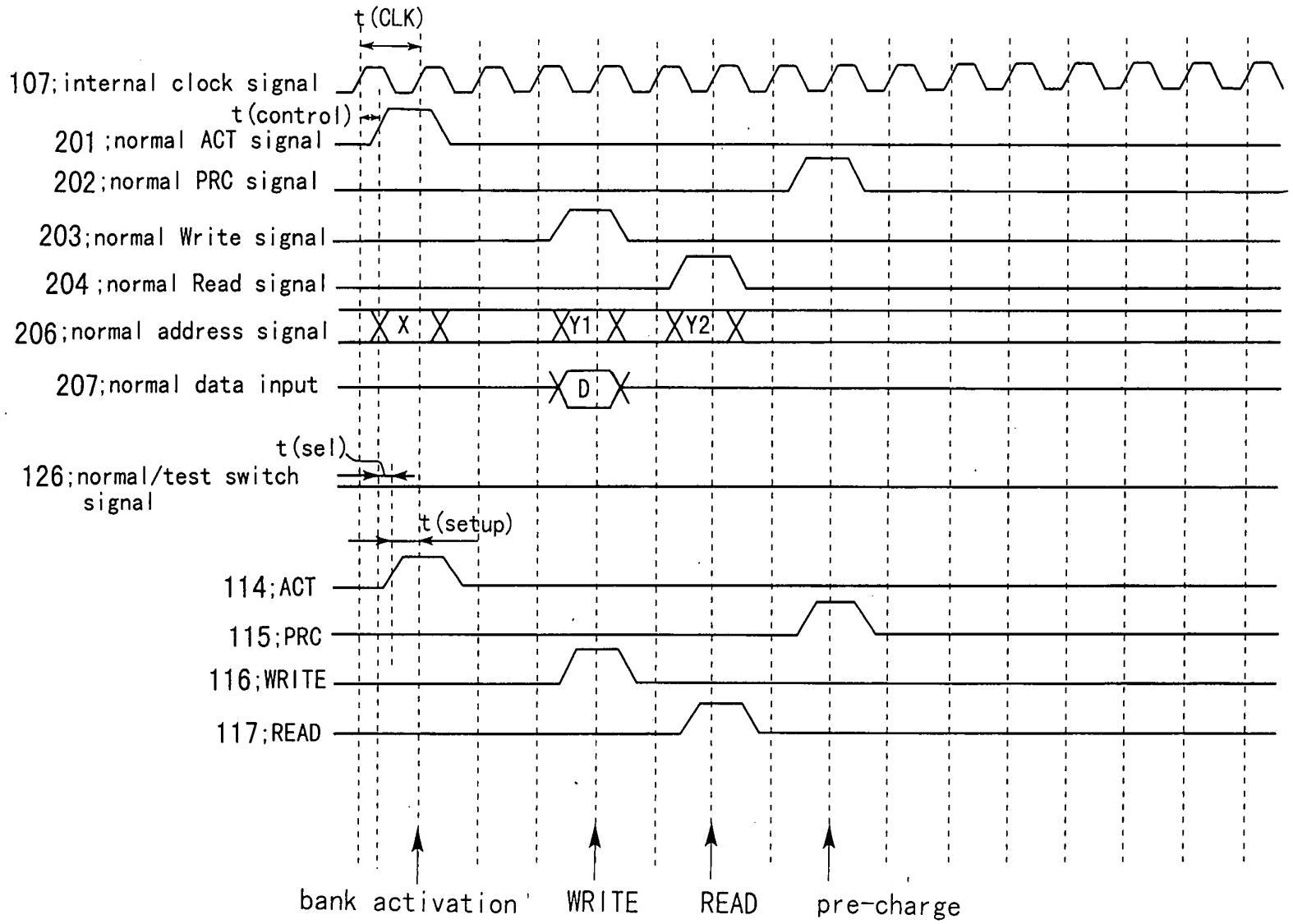
t(CLK)
107;internal clock signal
t(control)
201;normal ACT signal
202;normal PRC signal
203;normal Write signal
204;normal Read signal
206;normal address signal
X
Y1
Y2
207;normal data input
D
t(sel)
126;normal/test switch signal
t(setup)
114;ACT
115;PRC
116;WRITE
117;READ
bank activation
WRITE
READ
pre-charge

FIG. 5

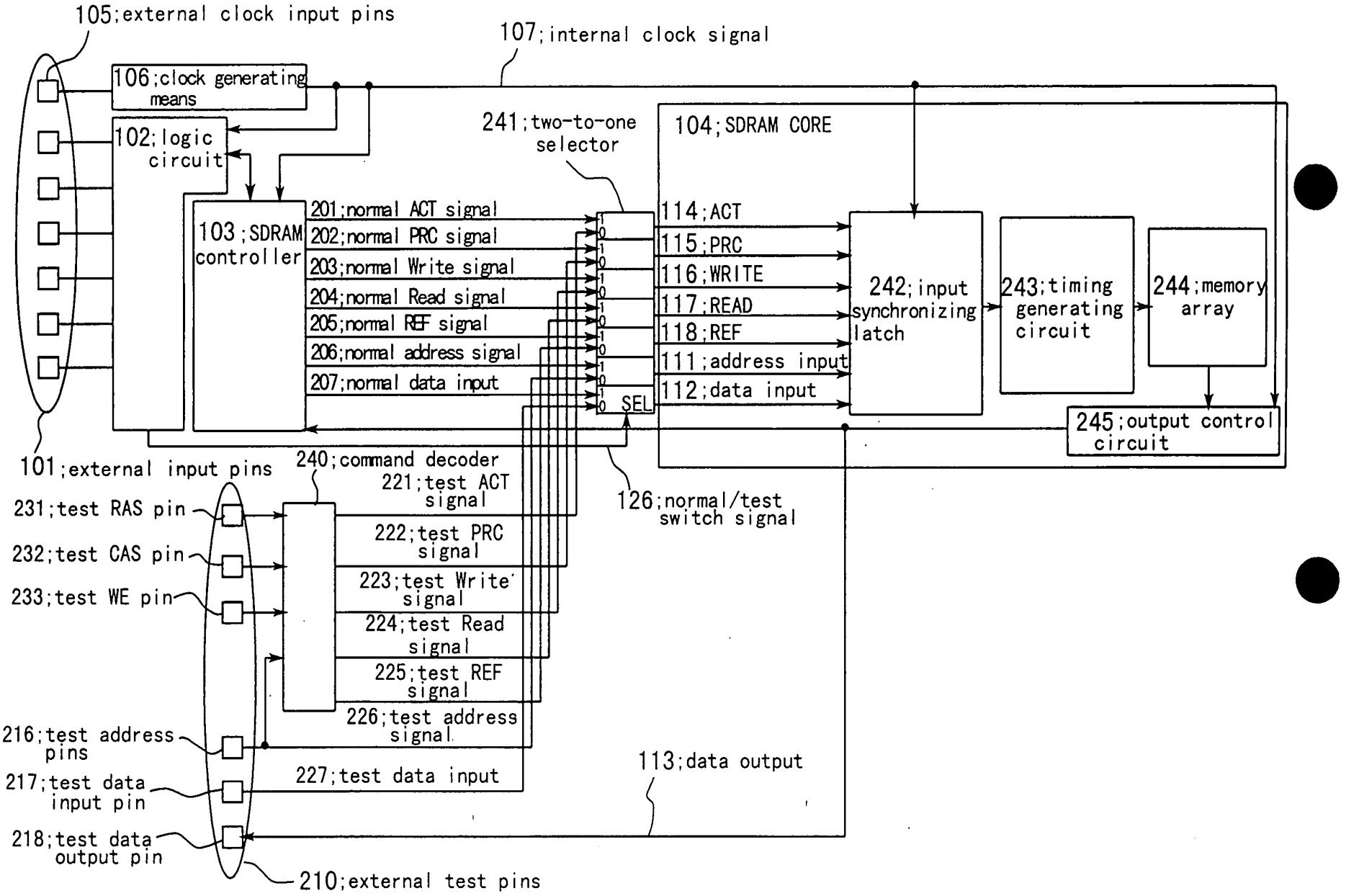

FIG. 6

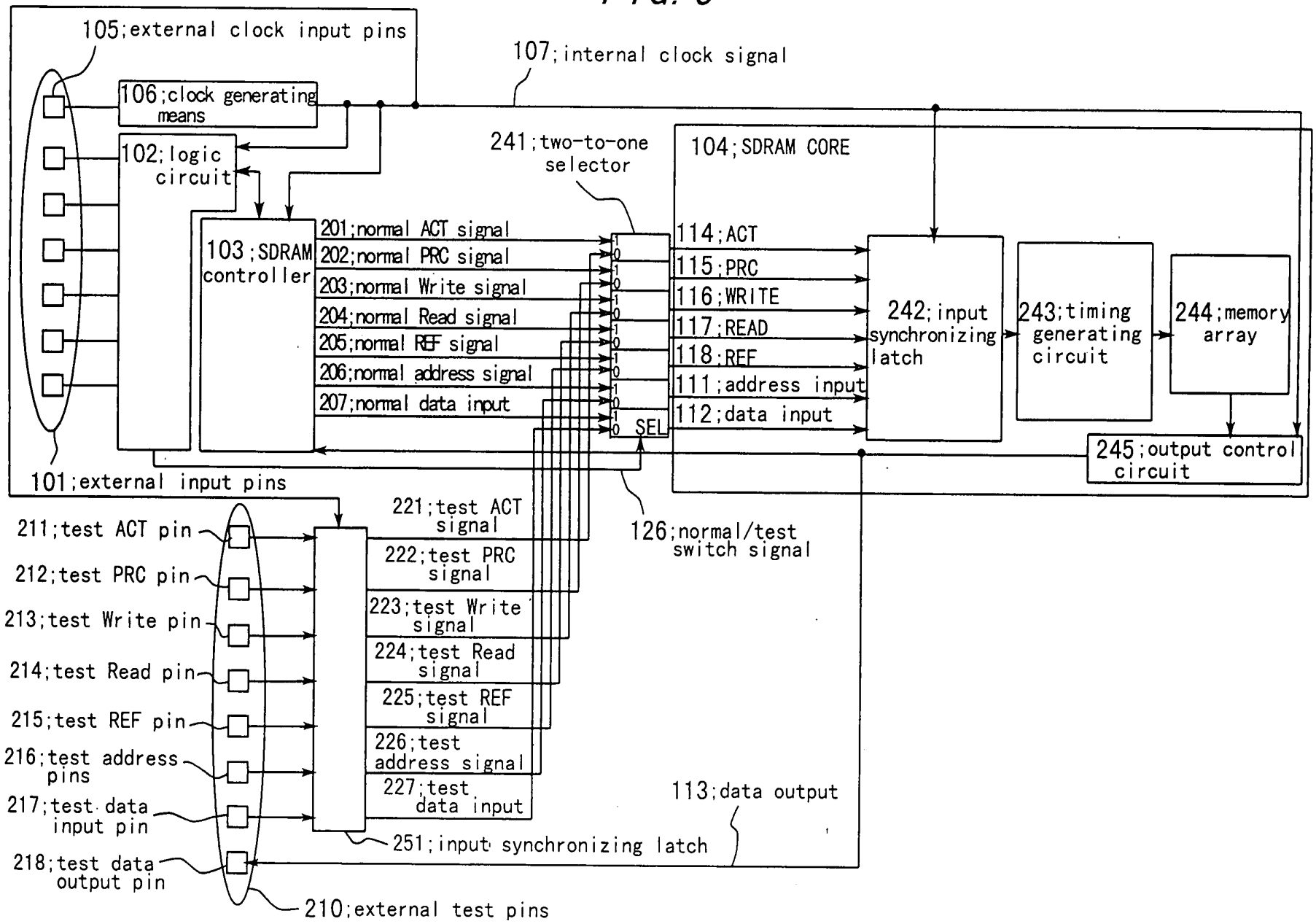
105;external clock input pins
107;internal clock signal
106;clock generating means
102;logic circuit
241;two-to-one selector
104;SDRAM CORE
103;SDRAM controller
201;normal ACT signal
202;normal PRC signal
203;normal Write signal
204;normal Read signal
205;normal REF signal
206;normal address signal
207;normal data input
SEL
114;ACT
115;PRC
116;WRITE
117;READ
118;REF
111;address input
112;data input
242;input synchronizing latch
243;timing generating circuit
244;memory array
245;output control circuit
101;external input pins
126;normal/test switch signal
211;test ACT pin
212;test PRC pin
213;test Write pin
214;test Read pin
215;test REF pin
216;test address pins
217;test data input pin
218;test data output pin
221;test ACT signal
222;test PRC signal
223;test Write signal
224;test Read signal
225;test REF signal
226;test address signal
227;test data input
113;data output
251;input synchronizing latch
210;external test pins

FIG. 7

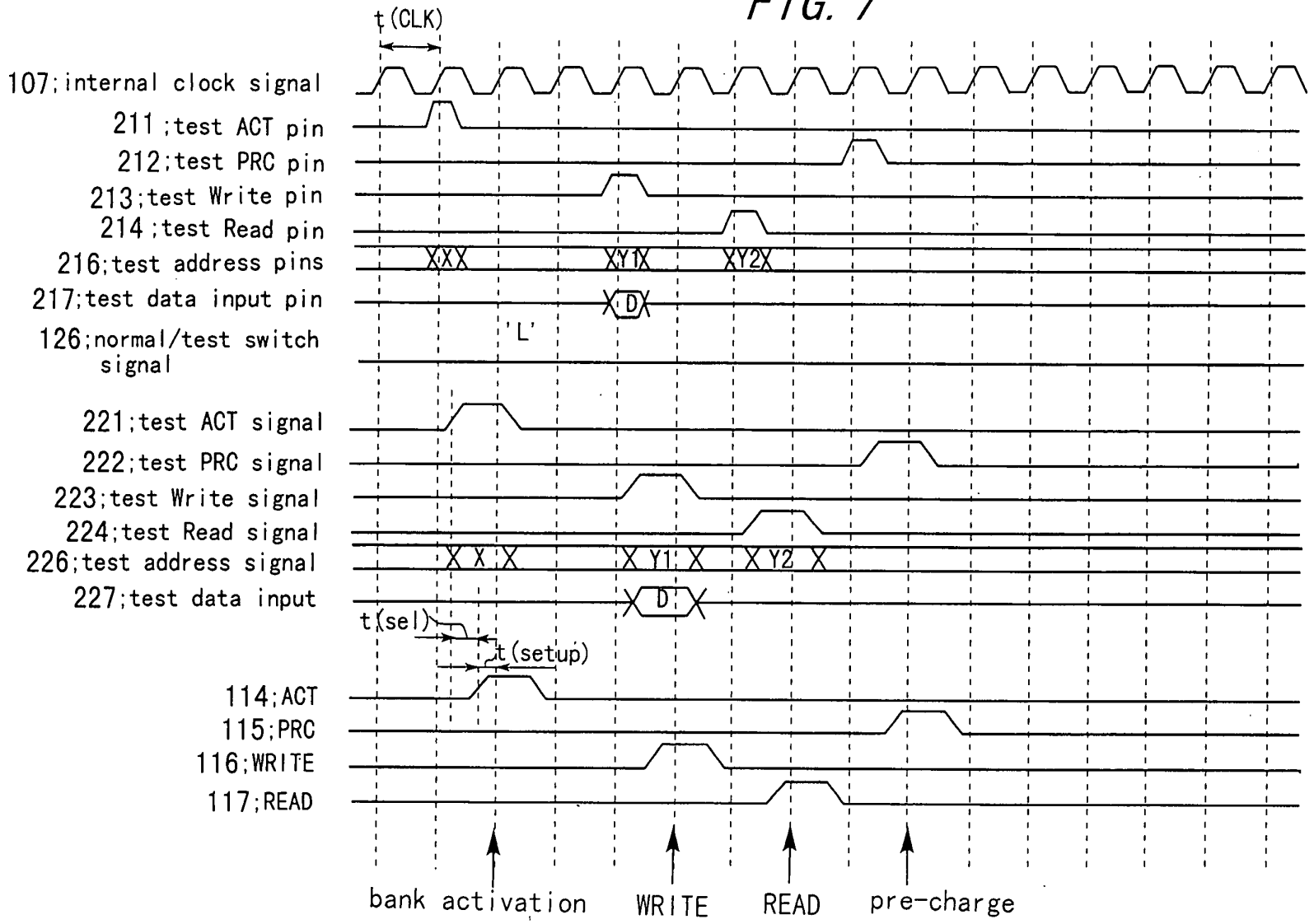
t(CLK)
107;internal clock signal
211 ;test ACT pin
212;test PRC pin
213;test Write pin
214 ;test Read pin
216;test address pins
217;test data input pin
126;normal/test switch signal
'L'
221;test ACT signal
222;test PRC signal
223;test Write signal
224;test Read signal
226;test address signal
227;test data input
X
Y1
Y2
D
t(sel)
t(setup)
114;ACT
115;PRC
116;WRITE
117;READ
bank activation
WRITE
READ
pre-charge

FIG. 8

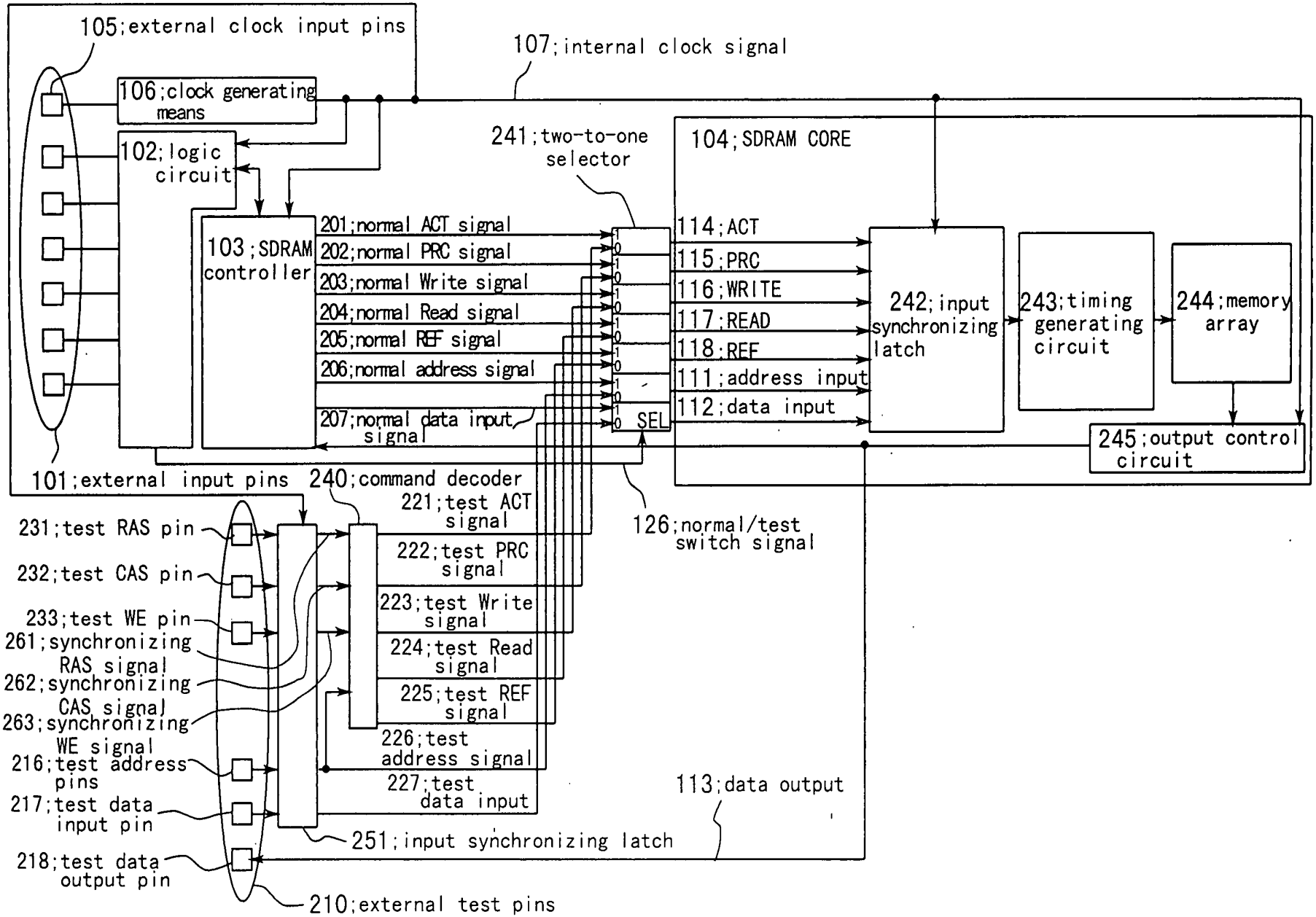
105;external clock input pins
107;internal clock signal
106;clock generating means
102;logic circuit
241;two-to-one selector
104;SDRAM CORE
103;SDRAM controller
201;normal ACT signal
202;normal PRC signal
203;normal Write signal
204;normal Read signal
205;normal REF signal
206;normal address signal
207;normal data input signal
SEL
114;ACT
115;PRC
116;WRITE
117;READ
118;REF
111;address input
112;data input
242;input synchronizing latch
243;timing generating circuit
244;memory array
245;output control circuit
101;external input pins
240;command decoder
126;normal/test switch signal
231;test RAS pin
232;test CAS pin
233;test WE pin
261;synchronizing RAS signal
262;synchronizing CAS signal
263;synchronizing WE signal
216;test address pins
217;test data input pin
218;test data output pin
221;test ACT signal
222;test PRC signal
223;test Write signal
224;test Read signal
225;test REF signal
226;test address signal
227;test data input
113;data output
251;input synchronizing latch
210;external test pins

FIG. 9

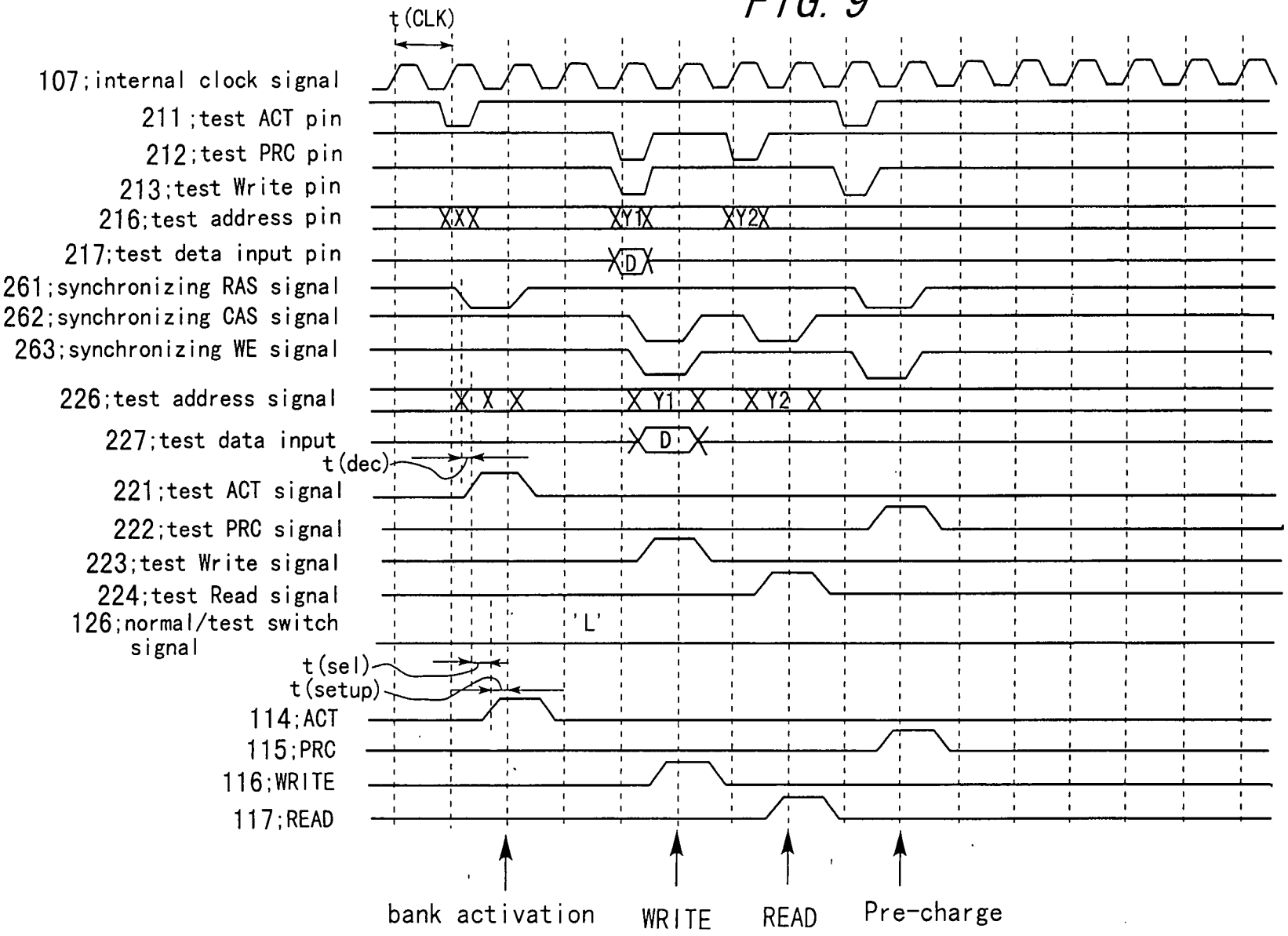
t(CLK)
107;internal clock signal
211;test ACT pin
212;test PRC pin
213;test Write pin
216;test address pin
217;test deta input pin
261;synchronizing RAS signal
262;synchronizing CAS signal
263;synchronizing WE signal
226;test address signal
227;test data input
t(dec)
221;test ACT signal
222;test PRC signal
223;test Write signal
224;test Read signal
126;normal/test switch signal
'L'
t(sel)
t(setup)
114;ACT
115;PRC
116;WRITE
117;READ
XXX
XY1X
XY2X
D
X X X
X Y1 X
X Y2 X
D
bank activation
WRITE
READ
Pre-charge

FIG. 10

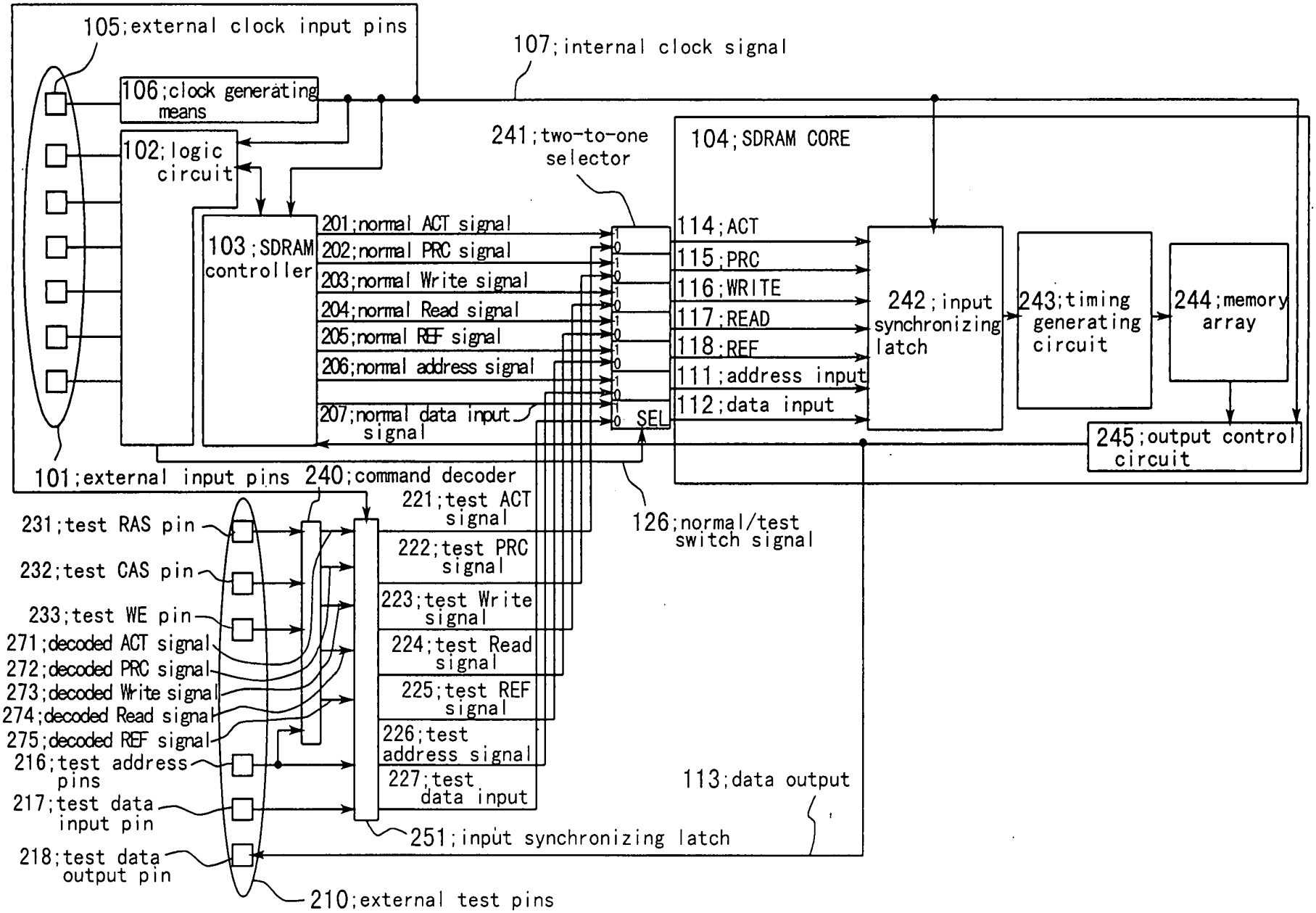
105;external clock input pins
107;internal clock signal
106;clock generating means
102;logic circuit
241;two-to-one selector
104;SDRAM CORE
103;SDRAM controller
201;normal ACT signal
202;normal PRC signal
203;normal Write signal
204;normal Read signal
205;normal REF signal
206;normal address signal
207;normal data input signal
SEL
114;ACT
115;PRC
116;WRITE
117;READ
118;REF
111;address input
112;data input
242;input synchronizing latch
243;timing generating circuit
244;memory array
245;output control circuit
101;external input pins
240;command decoder
126;normal/test switch signal
231;test RAS pin
232;test CAS pin
233;test WE pin
271;decoded ACT signal
272;decoded PRC signal
273;decoded Write signal
274;decoded Read signal
275;decoded REF signal
216;test address pins
217;test data input pin
218;test data output pin
221;test ACT signal
222;test PRC signal
223;test Write signal
224;test Read signal
225;test REF signal
226;test address signal
227;test data input
251;input synchronizing latch
113;data output
210;external test pins

FIG. 11

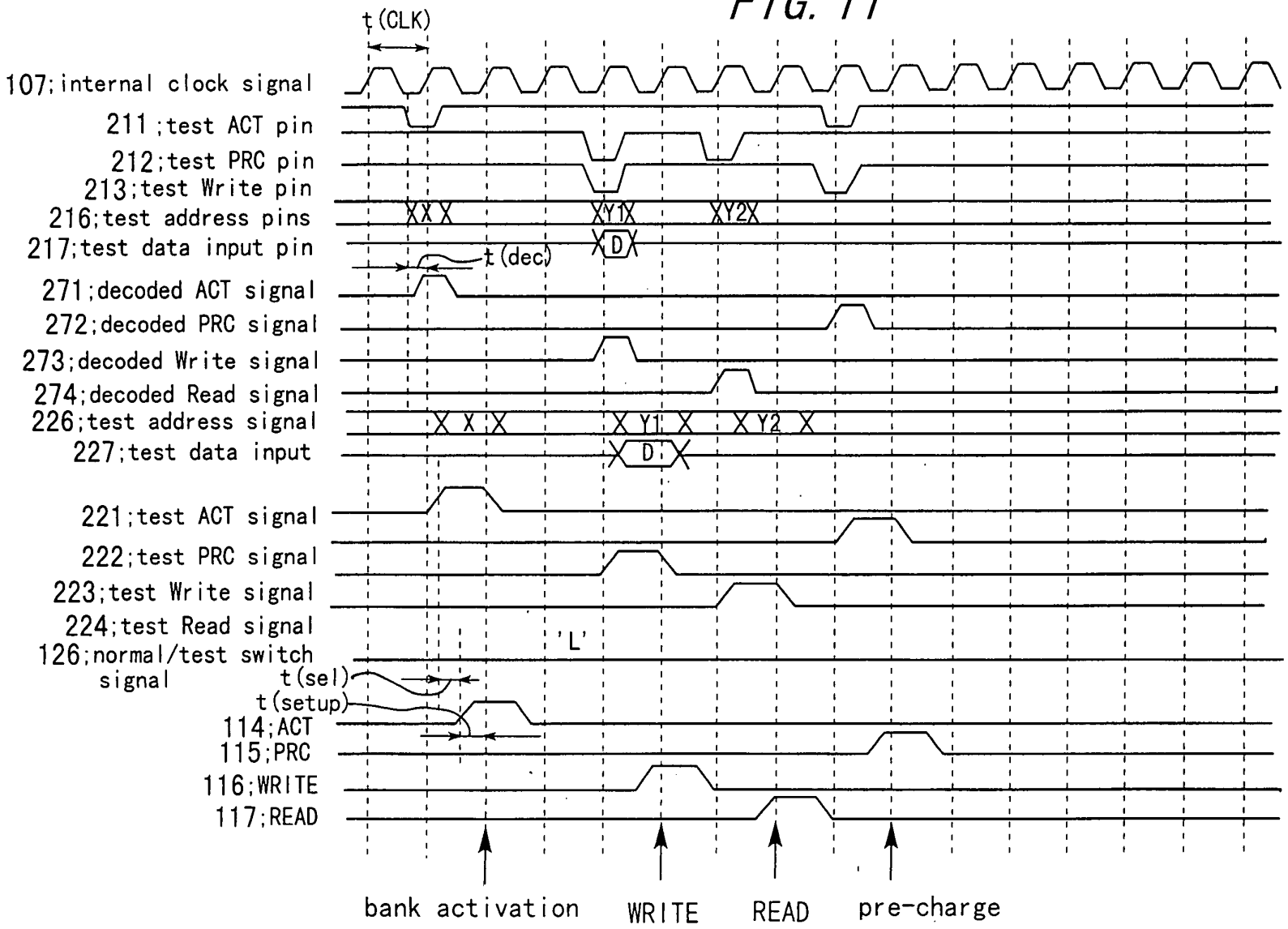
t(CLK)
107;internal clock signal
211;test ACT pin
212;test PRC pin
213;test Write pin
216;test address pins
217;test data input pin
t(dec)
271;decoded ACT signal
272;decoded PRC signal
273;decoded Write signal
274;decoded Read signal
226;test address signal
227;test data input
221;test ACT signal
222;test PRC signal
223;test Write signal
224;test Read signal
126;normal/test switch signal
'L'
t(sel)
t(setup)
114;ACT
115;PRC
116;WRITE
117;READ
X
Y1
Y2
D
bank activation
WRITE
READ
pre-charge

FIG. 12 Prior Art

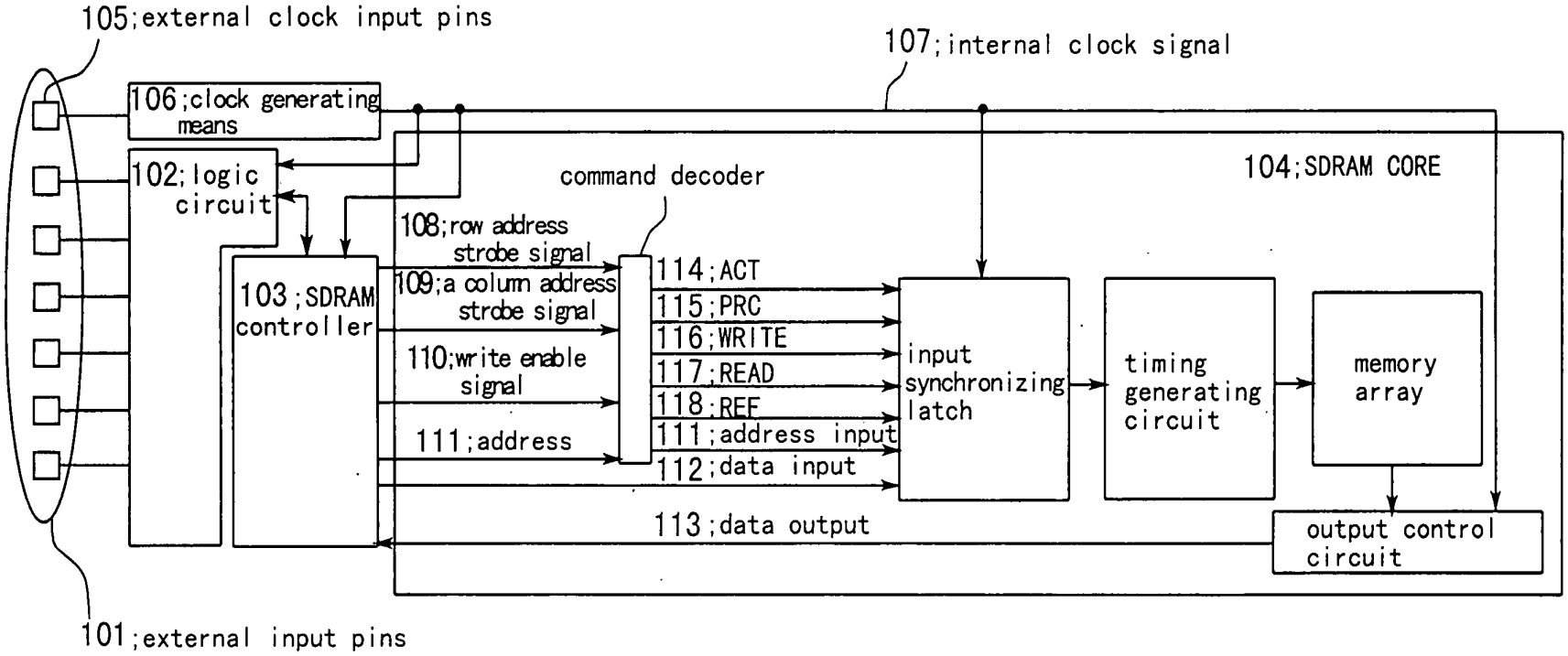

FIG. 13 Prior Art

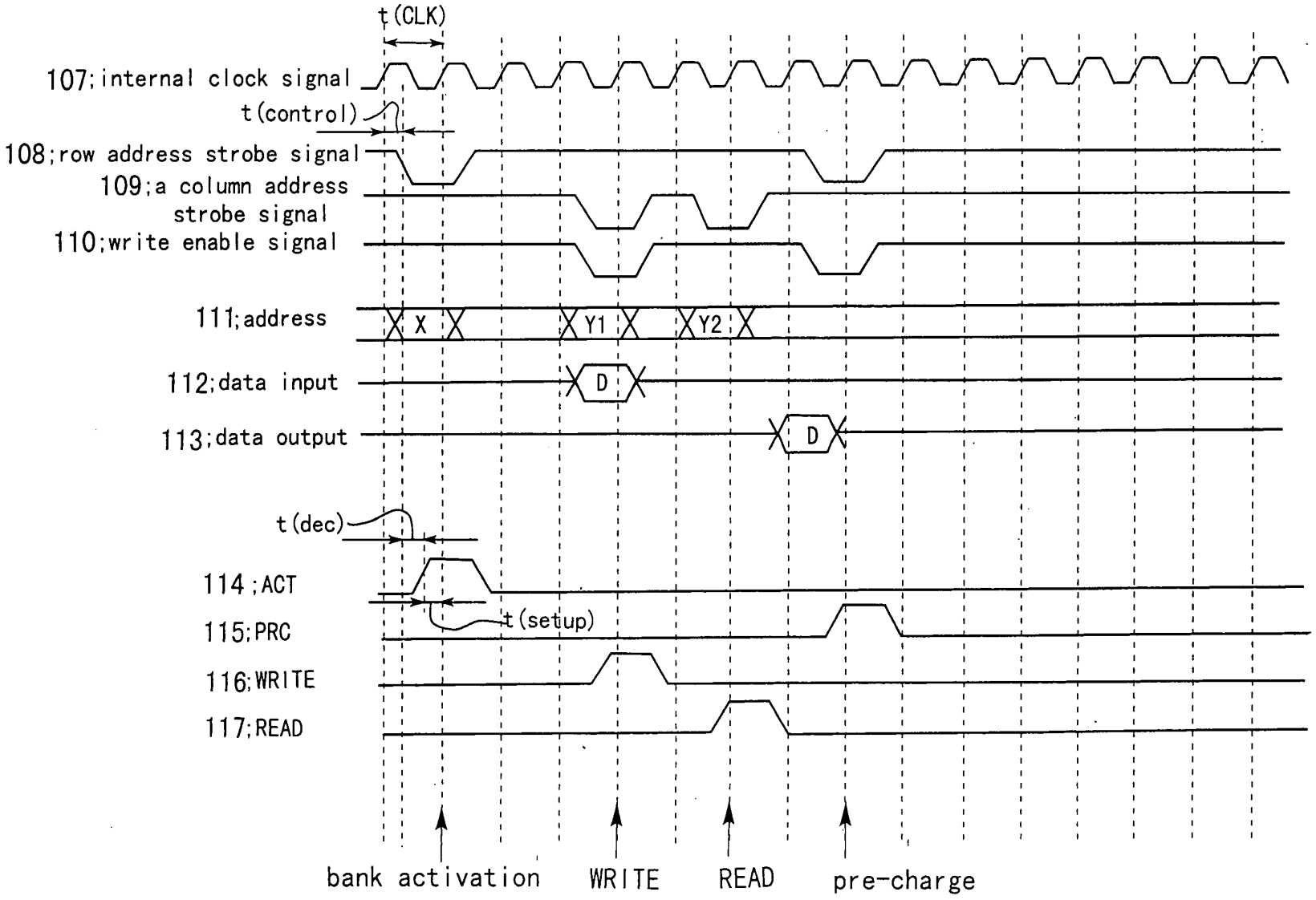

FIG. 14 Prior Art